AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1.(original) An encoder comprising:

a changing-point counter for counting changing points of n-bit data(n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

a code converter for converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the discrimination bit is true; and

a parallel-to-serial converter for converting (n + 1)-bit data to a (n + 1)-bit serial code, the (n + 1)-bit data being generated by adding the discrimination bit to an output of the code converter.

2.(original) The encoder according to claim 1, wherein the discrimination bit is added to the (n + 1)-bit data as its first or last bit.

3.(original) The encoder according to claim 1, wherein even- or odd- numbered bits of the n-bit serial data are inverted when the discrimination bit is true.

4.(original) The encoder according to claim 1, wherein the changing-point counter conducts its counting operation for (n + 1)-bit data generated by adding a last bit of an immediately

preceding n-bit serial code the encoder has dealt to the n-bit serial data.

5.(original) The encoder according to claim 2, wherein the n-bit serial data has an odd bit number and the discrimination bit is added to the (n +1)-bit serial code as its last bit;

and wherein when a last bit of the n-bit serial data is not a bit for conversion of the code converter, the counting result is equal to the predetermined value, and the last bit of the n-bit serial data is true, the discrimination bit is set to be true.

6.(original) The encoder according to claim 1, wherein the predetermined value is a largest integer equal to or less than (1/2) x (a bit number of the n-bit serial data - 1).

7.(original) An encoder comprising:

a parallel-to-serial converter for converting n-bit data (n: a positive integer) to n-bit serial data;

a changing-point counter for counting changing points of the n-bit serial data to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

a code converter for converting the n-bit serial data to a (n +1)-bit serial code in such a way that bist of the n-bit serial data located at predetermined positions are inverted when the discrimination bit is true; and

the (n +1)-bit serial code being generated by adding the discrimination bit to the n-bit serial data.

8.(original) The encoder according to claim 7, wherein the discrimination bit is added to the (n + 1)-bit data as its first or last bit.

9.(original) The encoder according to claim 7, wherein even- or odd- numbered bits of the n-bit serial data are inverted when the discrimination bit is true.

10.(original) The encoder according to claim 7, wherein the changing point counter conducts its counting operation for (n +1)-bit data generated by adding a last bit of an immediately preceding n-bit serial code the encoder has dealt to the n-bit serial data.

11.(original) The encoder according to claim 8, wherein the n-bit serial data has an odd bit number and the discrimination bit is added to the (n +1)-bit serial code as its last bit;

and wherein when a last bit of the n-bit serial data is not a bit for conversion of the code converter, the counting result is equal to the predetermined value, and the last bit of the n-bit serial data is true, the discrimination bit is set to be true.

12.(original) The encoder according to claim 7, wherein the predetermined value is a largest integer equal to or less than (1/2) x (a bit number of the n-bit serial data - 1).

13.(currently amended) A decoder comprising:

a serial-to-parallel converter for converting the (n +1)-bit serial code generated by the encoder according to claim 1 [[or 7]] to a (n +1)-bit parallel data; and

a code deconverter for deconverting the (n +1)-bit parallel data in such a way that some of the n-bits of the (n+1)-bit parallel data located at predetermined positions excluding the

discrimination bit are inverted when the discrimination bit is true.

14.(currently amended) A decoder comprising:

a code deconverter for inverting the (n + 1)-bit serial code generated by the encoder according to claim 1 [[or 7]] in such a way that some of the n-bits of the (n + 1)-bit serial code located at predetermined positions excluding the discrimination bit are inverted when the discrimination bit is true, thereby outputting a n-bit serial data; and

a serial-to-parallel converter for converting the n-bit serial data to a n-bit parallel data.

15.(currently amended) A data transfer system comprising:

(a) an encoder including a changing-point counter, a code converter, and a parallel-to-serial converter;

the changing-point counter counting changing points of n-bit data (n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

the code converter converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the discrimination bit is true; and

the parallel-to-serial converter converting (n + 1)-bit data to a (n + 1)-bit serial code, the (n + 1)-bit data being generated by adding the discrimination bit to an output of the code converter; and

(b) a decoder including a serial-to-parallel converter and a code deconverter;

the serial-to-parallel converter converting the (n +1)-bit serial code generated by the encoder according to claim 1 [[or 7]] to a (n +1)-bit parallel data; and

the code deconverter deconverting the (n + 1)-bit parallel data in such a way that some of the n-bits of the (n +1)-bit parallel data located at predetermined positions excluding the discrimination bit are inverted when the discrimination bit is true.

wherein the (n + 1)-bit serial code is serially transferred from the encoder to the decoder.

16.(currently amended) A data transfer system comprising:
(a) an encoder including a parallel-to-serial converter, a changing-point counter, and a code converter;

the parallel-to-serial converter converting n-bit data (n: a positive integer) to n-bit serial data;

the changing-point counter counting changing points of the n-bit serial data to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

the code converter converting the n-bit serial data to a (n + 1)-bit serial code in such a way that bits of the n-bit serial data located at predetermined positions are inverted when discrimination bit is true; and

the (n + 1)-bit serial code being generated by adding the discrimination bit to the n-bit serial data; and
(b) a decoder including a serial-to-parallel converter and a code deconverter;

the serial-to-parallel converter converting the (n + 1)-bit serial code generated by the encoder according to claim 1 [[or 7]] to a (n +1)-bit parallel data; and

the code deconverter deconverting the (n + 1)-bit parallel data in such a way that some of the n-bits of the (n + 1)-bit parallel data located at predetermined positions excluding the

discrimination bit are inverted when the discrimination bit is true;

wherein the (n + 1)-bit serial code is serially transferred from the encoder to the decoder.

17.(currently amended) A data transfer system comprising:

(a) an encoder including a changing-point counter, a code converter, and a parallel-to-serial converter;

the changing-point counter counting changing points of n-bit data (n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

the code converter converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the discrimination bit is true; and

the parallel-to-serial converter converting (n + 1)-bit data to a (n +1)-bit serial code, the (n + 1)-bit data being generated by adding the discrimination bit to an output of the code converter; and

(b) a decoder including a code deconverter and a serial-to-parallel converter;

the code deconverter deconverting the (n + 1)-bit serial code generated by the encoder according to claim 1 [[or 7]] in such a way that some of the n-bits of the (n + 1)-bit serial code located at predetermined positions excluding the discrimination bit are inverted when the discrimination bit is true, thereby outputting a n-bit data; and

the serial-to-parallel converter converting the n-bit serial data to a n-bit parallel data;

wherein the (n + 1)-bit serial code is serially transferred from the encoder to the decoder.

18.(currently amended) A data transfer system comprising:
(a) an encoder including a the parallel-to-serial converter, a changing-point counter, and a code converter;

the parallel-to serial converter converting n-bit data (n: a positive integer) to n-bit serial data;

the changing-point counter counting changing points of the n-bit serial data to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

the code converter converting the n-bit serial data to a (n + 1)-bit serial code in such a way that bits of the n-bit serial data located at predetermined positions are inverted when the discrimination bit is true; and

the (n + 1)-bit serial code being generated by adding the discrimination bit to the n-bit serial data; and
(b) a decoder including a code deconverter and a serial-to-parallel converter;

the code deconverter deconverting the (n + 1)-bit serial code generated by the encoder according to claim 1 [[or 7]] in such a way that some of the n-bits of the (n +1)-bit serial code located at predetermined positions excluding the discrimination bit are inverted when the discrimination bit is true, thereby outputting a n-bit data; and

the serial-to-parallel converter converting the n-bit serial data to a n-bit parallel data;

wherein the (n + 1)-bit serial code is serially transferred from the encoder to the decoder.

19.(original) A data transfer system comprising:
(a) a changing-point counter and a code converter located in a data transmission side;

the changing-point counter counting changing points of n-bit data (n: a positive integer) to generate a counting result, where values of adjoining bits change at each of the changing points;

the changing-point counter outputting a discrimination bit which is true when the counting result exceeds a predetermined value;

the code converter converting the n-bit data in such a way that bits of the n-bit data located at predetermined positions are inverted when the discrimination bit is true, thereby generating an inverted n-bit data; and

the code converter outputting a (n + 1)-bit serial code generated by adding the discrimination bit to the inverted n-bit data;

(b) a code deconverter located in a data reception side;

the code deconverter deconverting the (n + 1)-bit serial code outputted from the code converter in such a way that some of the n-bits of the (n + 1)-bit serial code located at predetermined positions excluding the discrimination bit are inverted when the discrimination bit is true;

wherein the (n + 1)-bit serial code is serially transferred from the data transmission side to the data reception side.

20.(original) The system according to claim 19, wherein the discrimination bit is added to the (n + 1)-bit serial code as its first or last bit.

21.(original) The system according to claim 19, wherein even- or odd- numbered ones of the n-bits of the (n + 1)-bit serial code excluding the discrimination bit are inverted when the discrimination bit is true.

22.(original) The system according to claim 19, wherein the changing-point counter conducts its counting operation for (n + 1)-bit serial code generated by adding a last bit of an

immediately preceding (n + 1)-bit serial code the data transmission side has dealt to the n-bits of the (n + 1)-bit serial code excluding the discrimination bit.

23.(original) The system according to claim 19, wherein the n-bits of the (n + 1)-bit serial code excluding the discrimination bit is odd;

and wherein the discrimination bit is added to the (n + 1)-bit serial code as its last bit;

and wherein when a last one of the n-bits of the (n + 1)-bit serial code is not a bit for conversion of the code converter, the counting result is equal to the predetermined value, and the last one of the n-bits of the (n + 1)-bit serial code is true, the discrimination bit is set to be true.

24.(original) The system according to claim 19, wherein the predetermined value is a largest integer equal to or less than (1/2) x (a bit number of the n-bit serial data - 1).